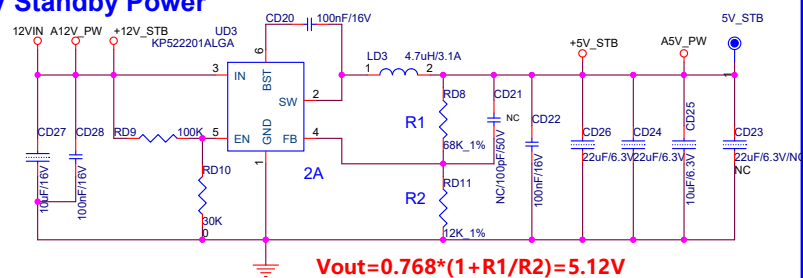
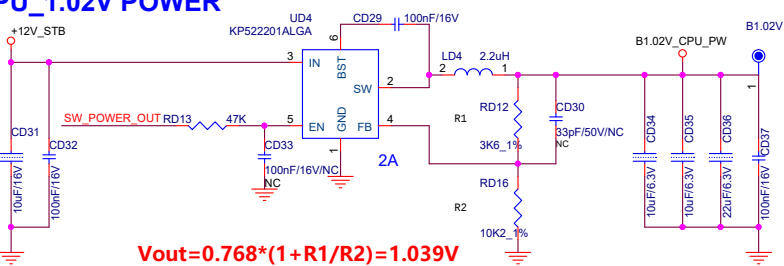


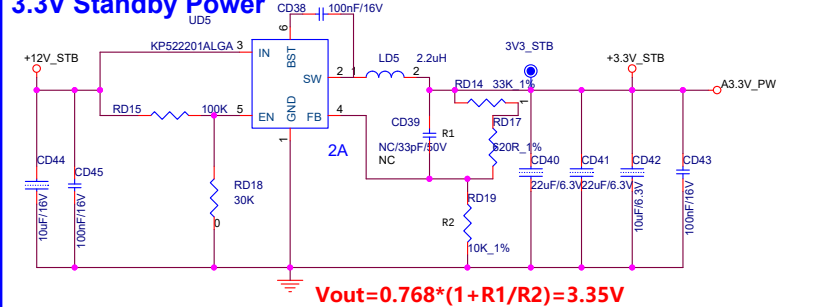
5V Standby Power



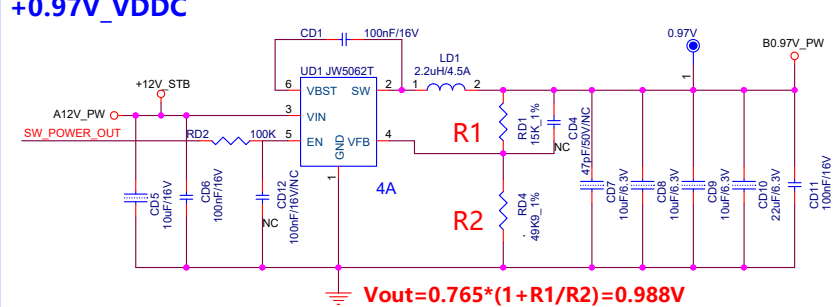
CPU_1.02V POWER



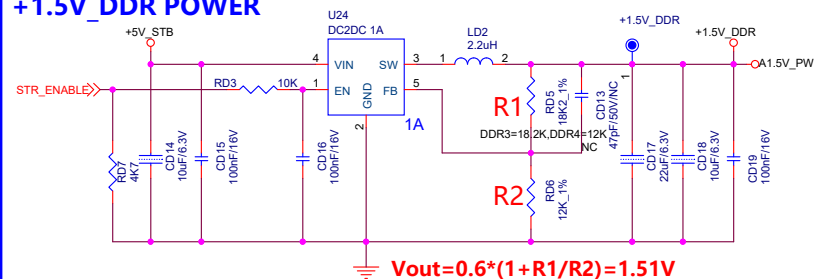
3.3V Standby Power



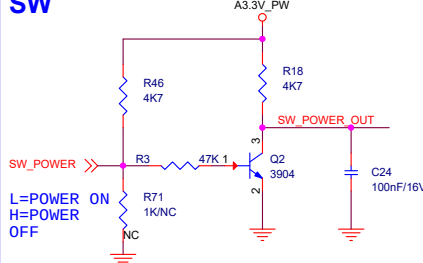
+0.97V VDDC



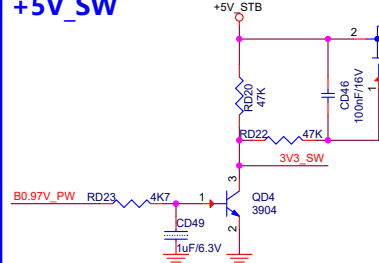
+1.5V_DDR POWER



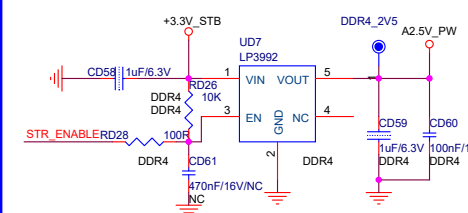
SW



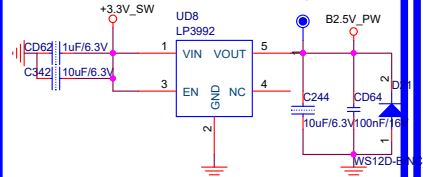
+5V_SW



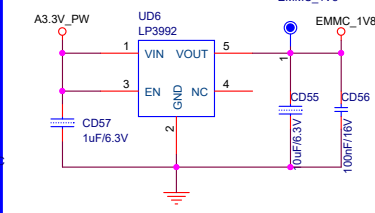
DDR4_2.5V



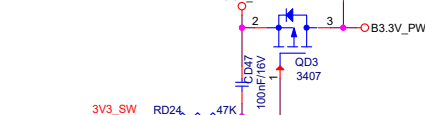
MAIN 2.5V

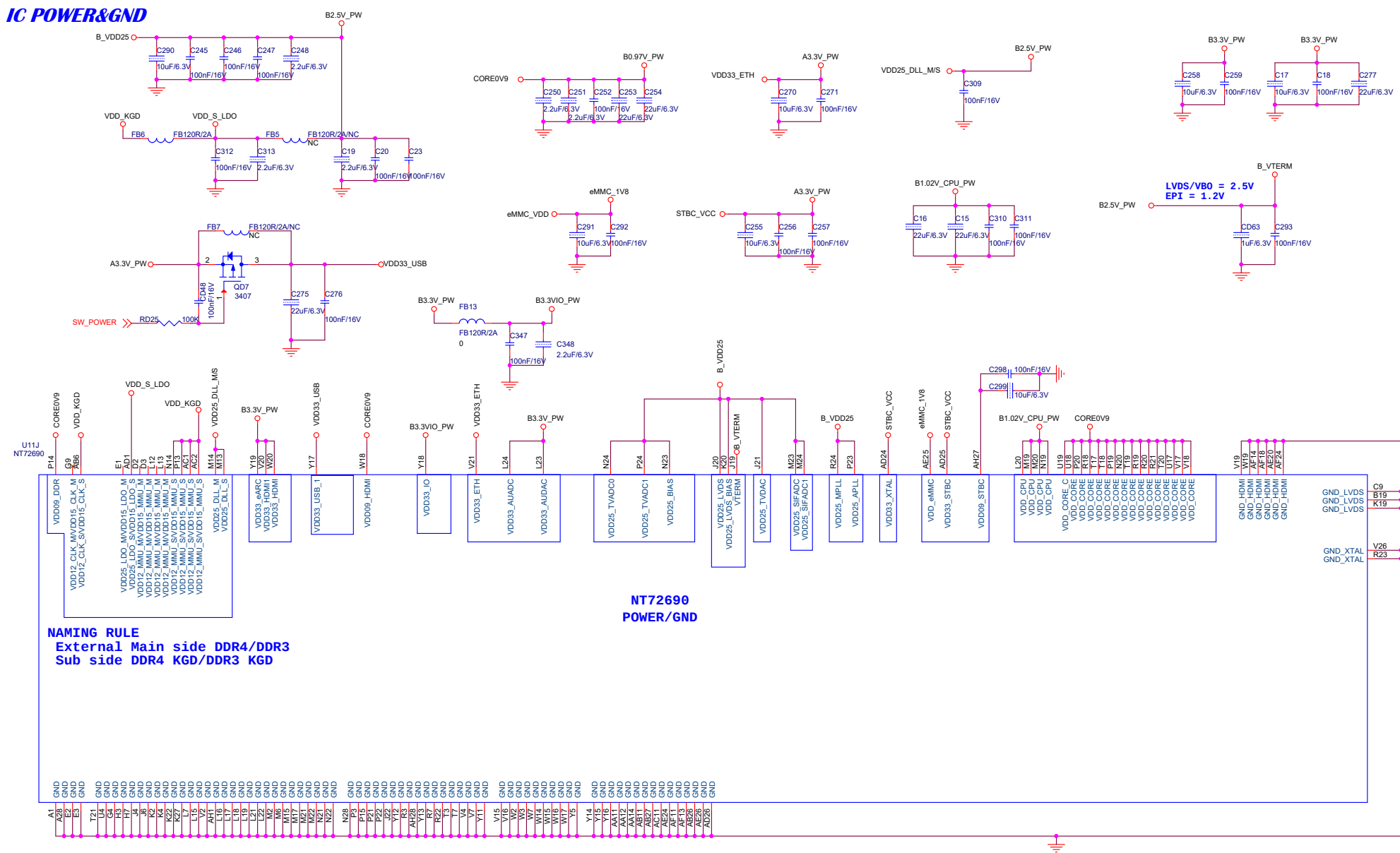


EMMC 1.8V



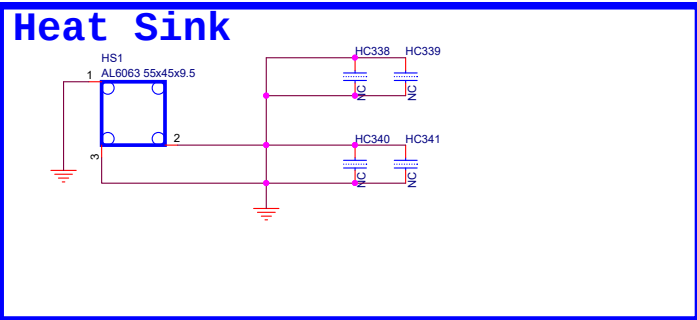
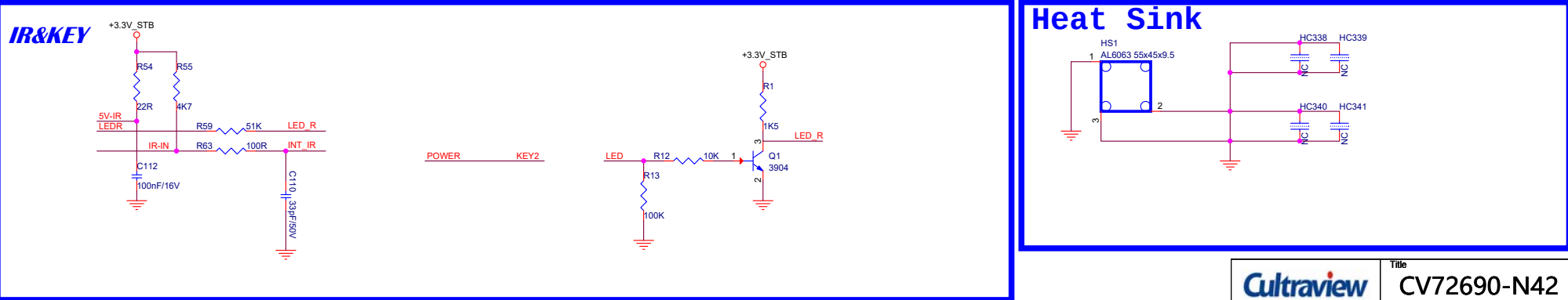
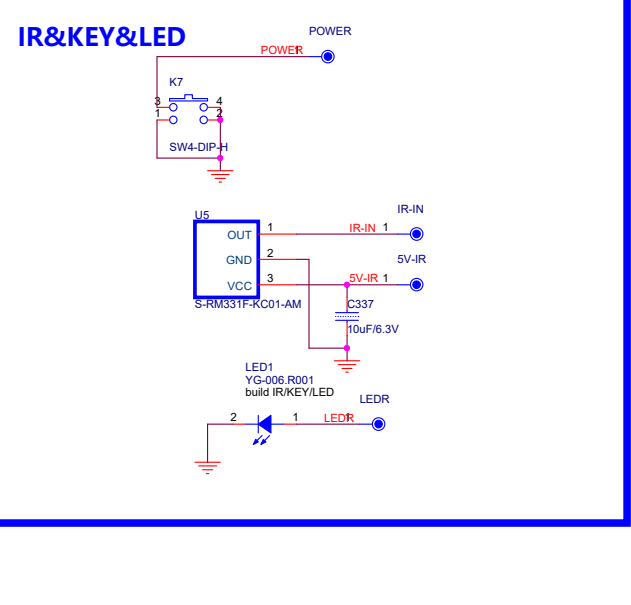
+3.3V_SW

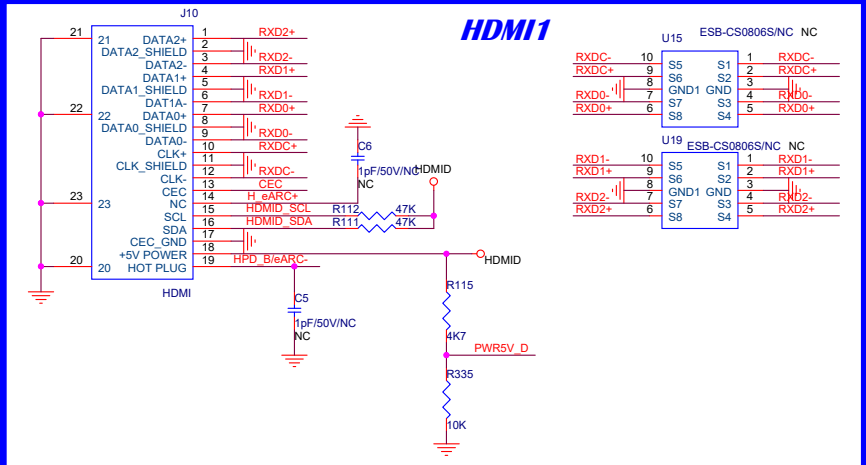
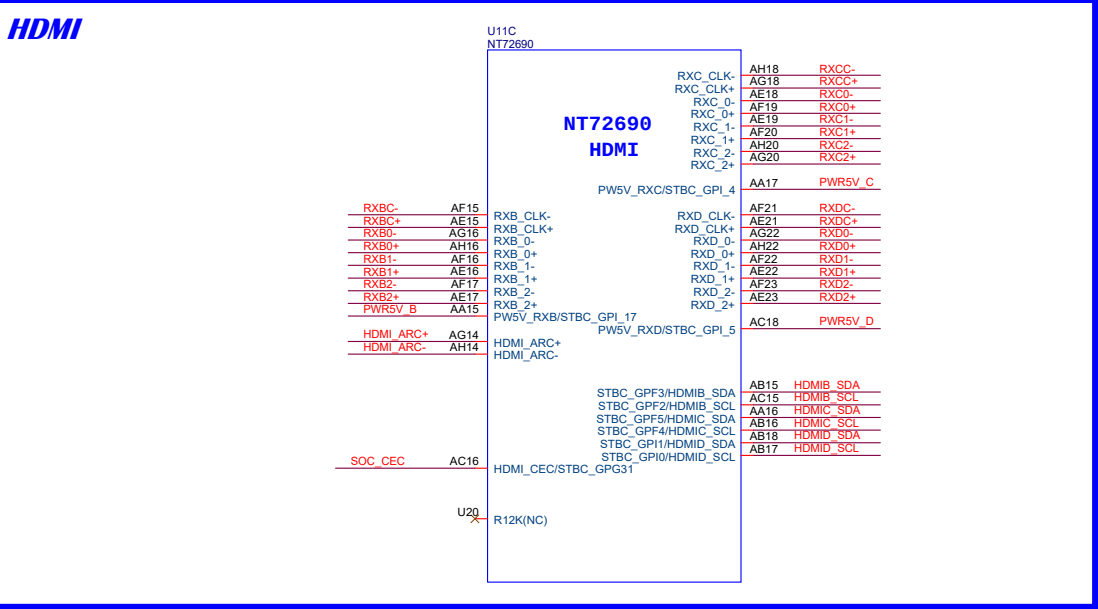
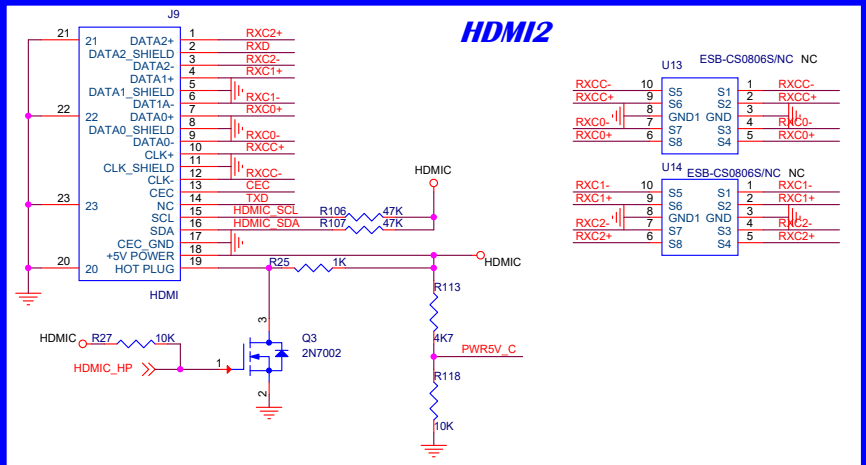
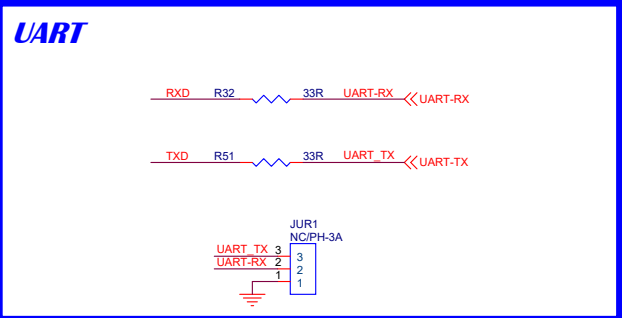
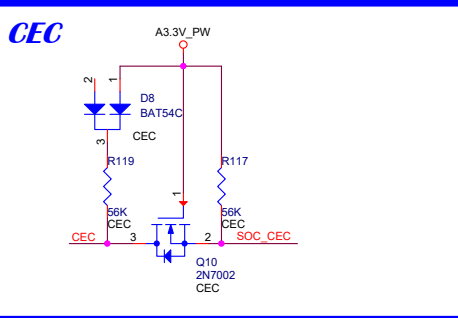
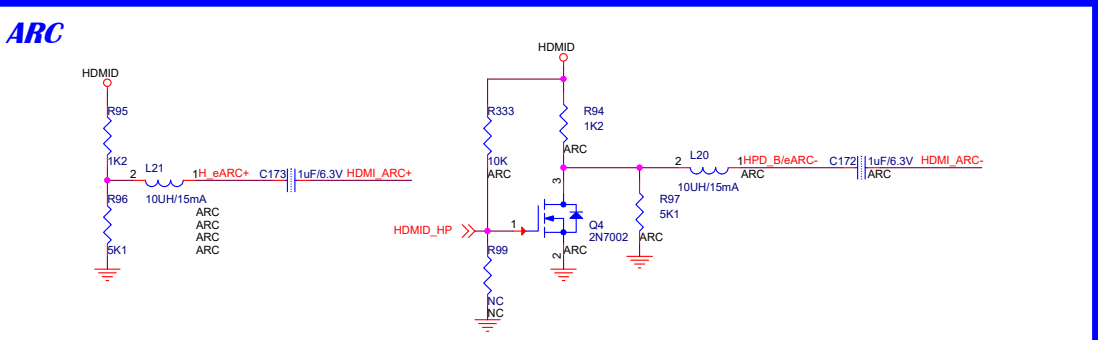
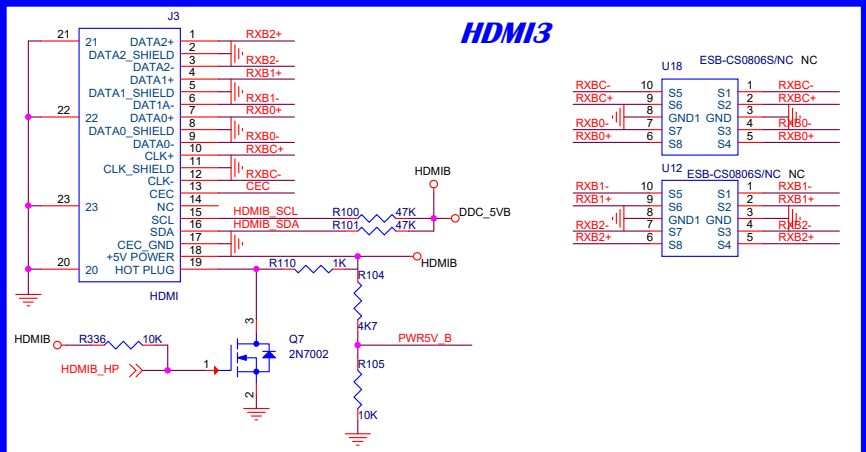


IC POWER&GND

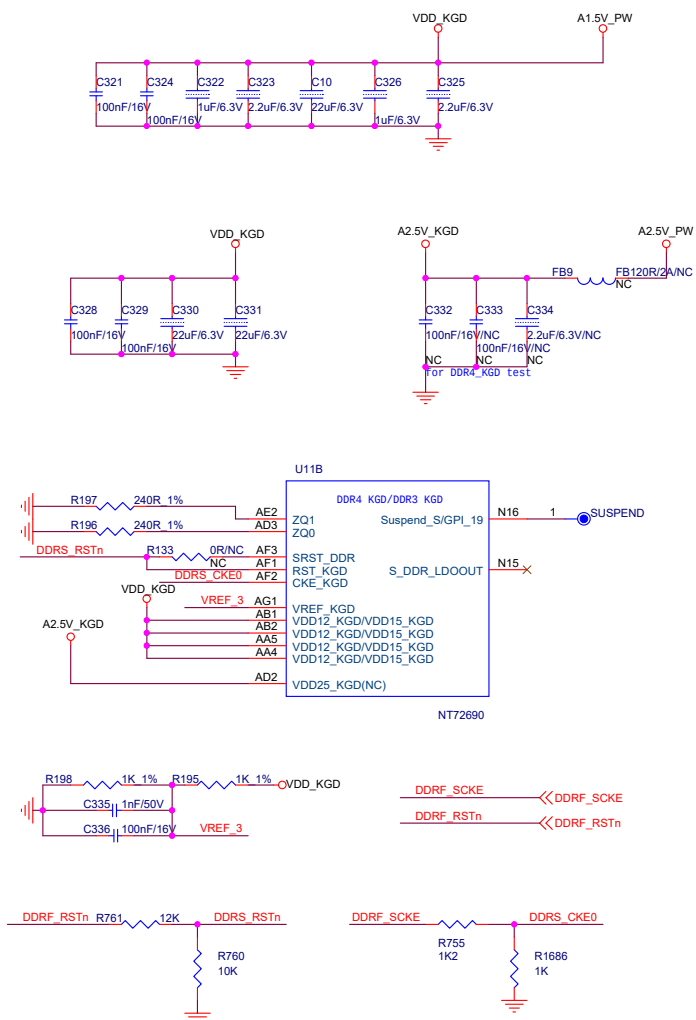
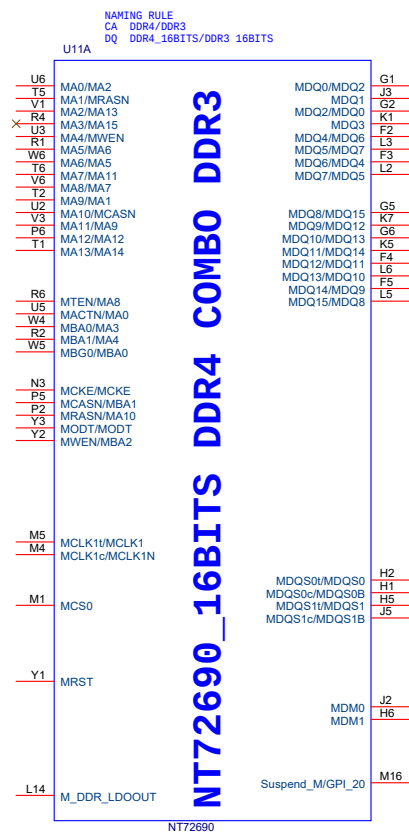
NAMING RULE
External Main side DDR4/DDR3
Sub side DDR4 KGD/DDR3 KGD

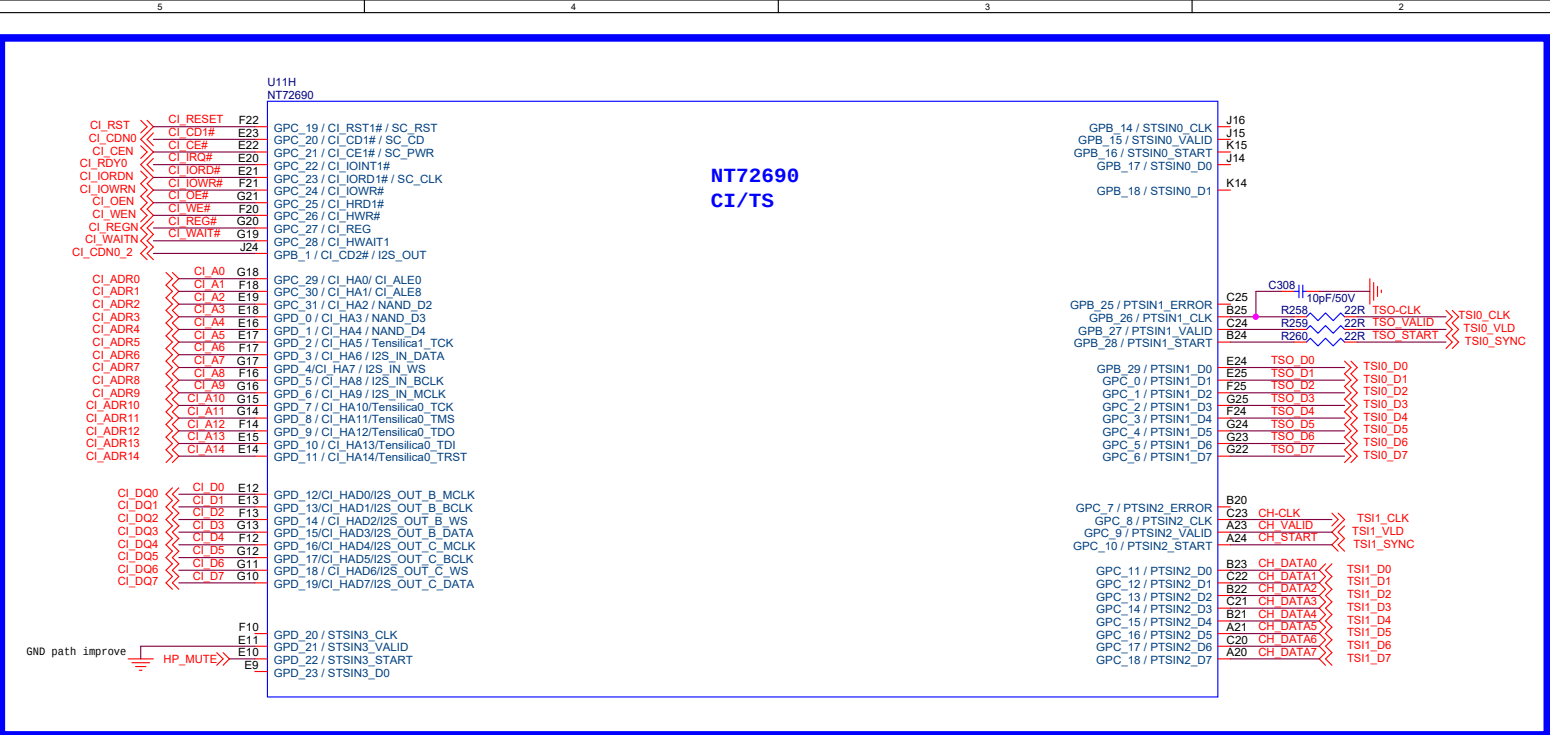
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DDR_S

**DDR_M**



CPU Side:

BS0_Bypass CPU MaskROM
0 : Using CPU MaskROM
1 : Bypass CPU MaskROM

eMMC:

BS13_eMMC bus width
BS13 =
0: EMMC Bus width is 8 bit
1: EMMC Bus width is 4 bit

BS15_eMMC ACK
0: Boot mode wait ACK
1: Boot mode do not wait ACK

BS18_eMMC clk_switch
0: 26M
1: 13M

STBC Side:

BS1_STBC Boot Strap Option
0: Boot from STBC
1: Boot from CPU, bypass STBC.

BS8_STBC watchdog
0: Default disable STBC watchdog
1: Default enable STBC watchdog

BS19_Internal boot strap for NF/eMMC type
0: NF/eMMC type internal boot strap enable
1: NF/eMMC type internal boot strap disable
(BS[7:6] = 00, BS8 is external; BS[17:16]=00,BS14=0, BS13,BS15,BS18 are external)

BS9_Security boot
0: no security boot
1: security boot

BS20_NAND I/O
0: NAND I/O in STBC eMMC side (BS12 = 1)
1: NAND I/O in ARM CI side (BS12 = 1, BS[4:3] = 00, 11)
or STBC SPI side (BS12 = 1, BS[4:3] = 01, 10)

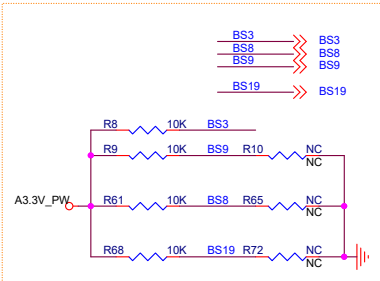
BS2_Bypass STBC MaskROM
When BS1=0,
0: Through STBC MaskROM
1: Bypass STBC MaskROM

BS12=0 , BS3,BS4_Device
BS4, 3 =
00: STBC boot from SPI, CPU boot from eMMC
01: STBC & CPU both boot from eMMC
10: STBC & CPU both boot from SPI
11: Reserved (same 00)

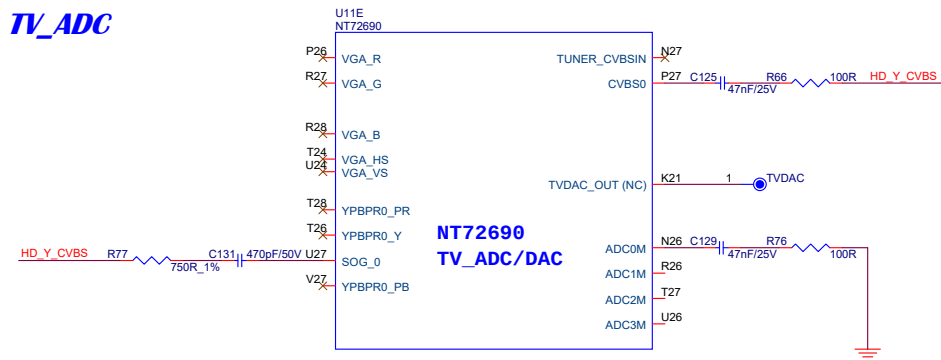
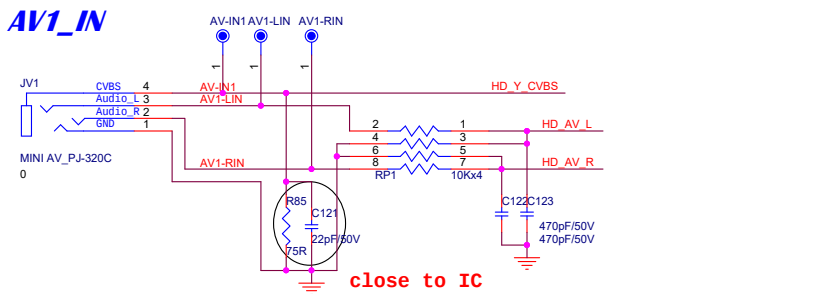
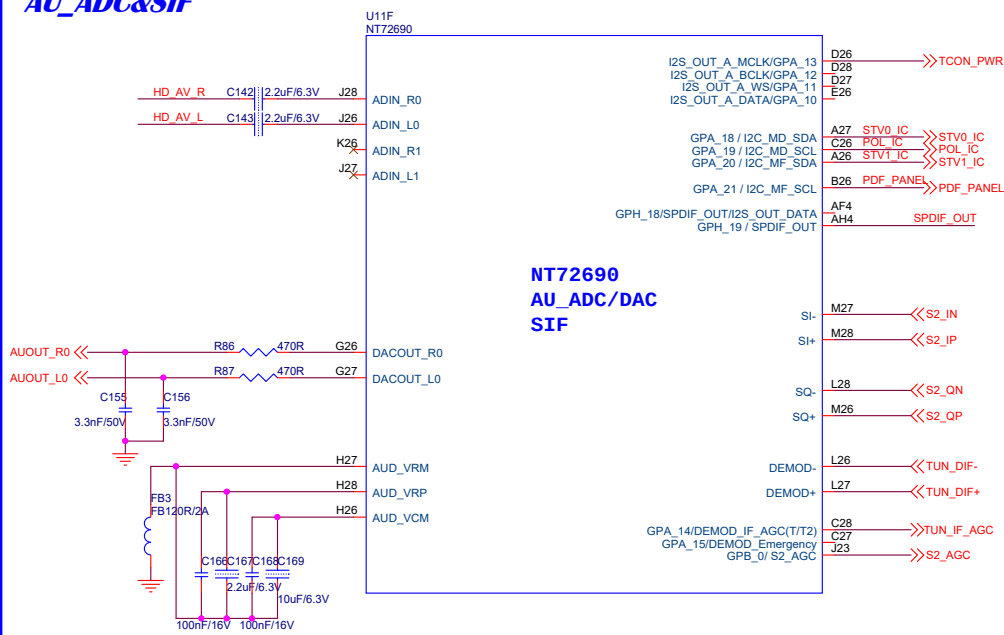
BS10_SPI Flash scramble
0: Disable
1: Enable

BS11_Turnkey Security
0: Disable
1: Enable

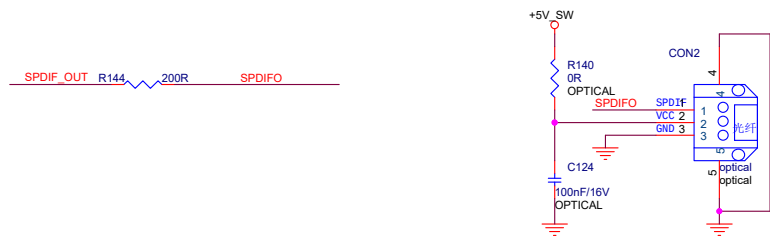
Internal Bootstrap

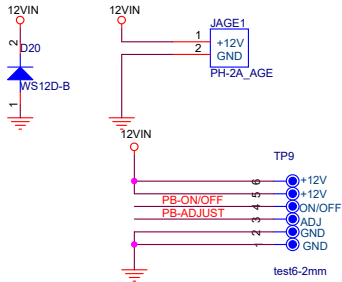
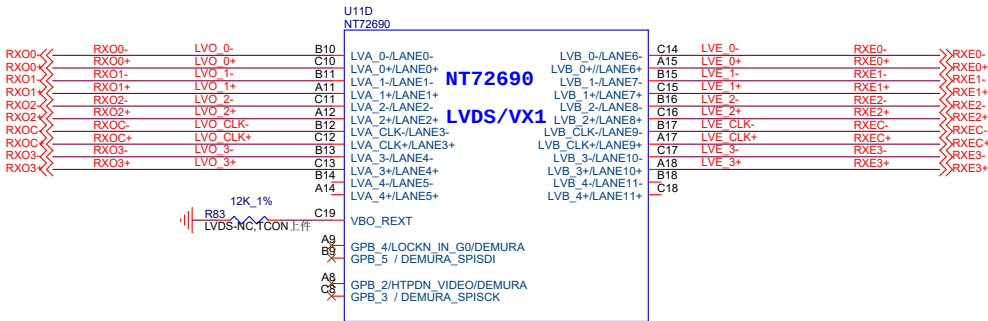


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		CV72690-N42	
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		07.CI/TS	
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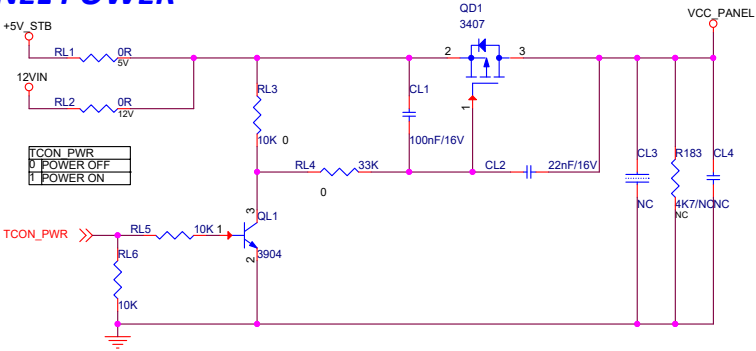
TV_ADC**AV1_IN*****AU_ADC&SIF***

SPDIF OUT

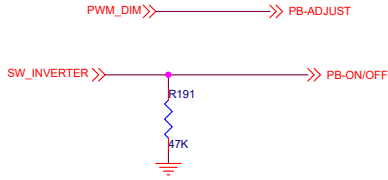




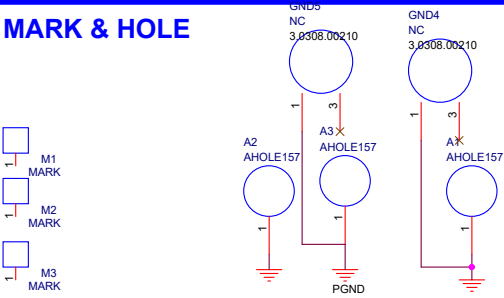
PANEL POWER



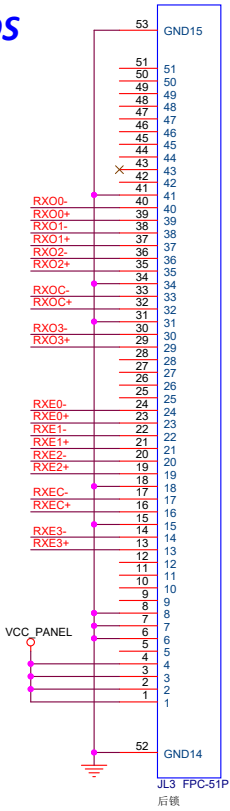
BackLight Controler



MARK & HOLE

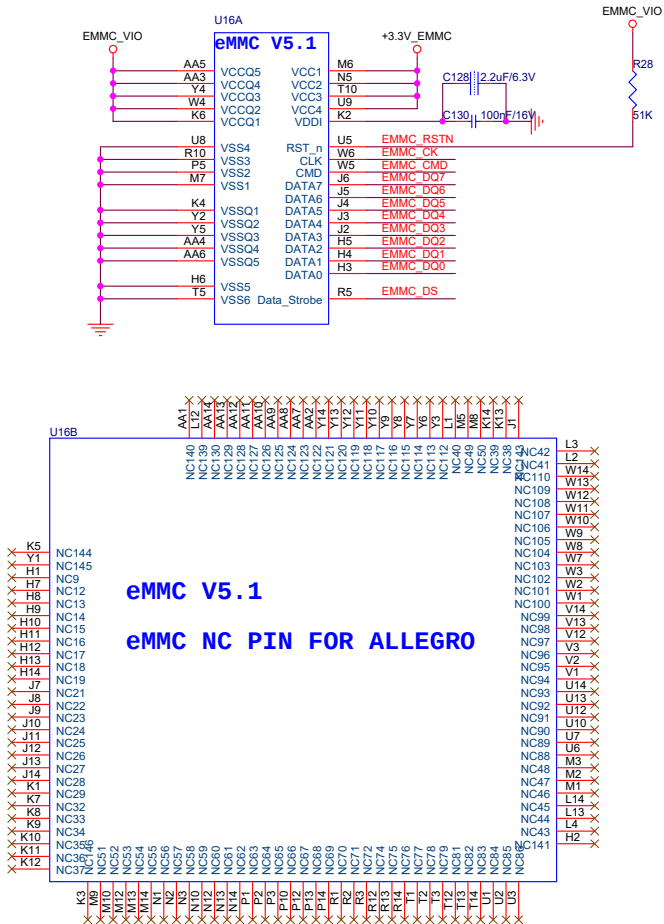


LVDS



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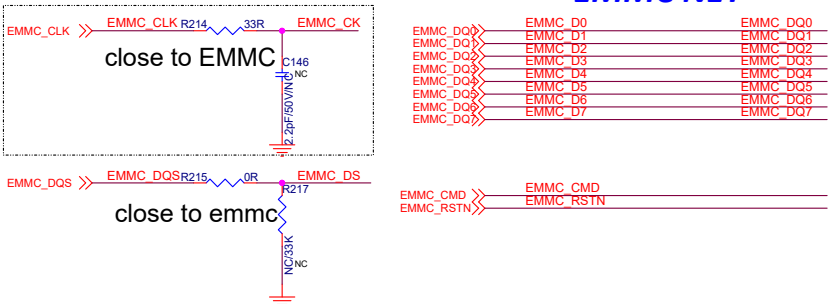
EMMC



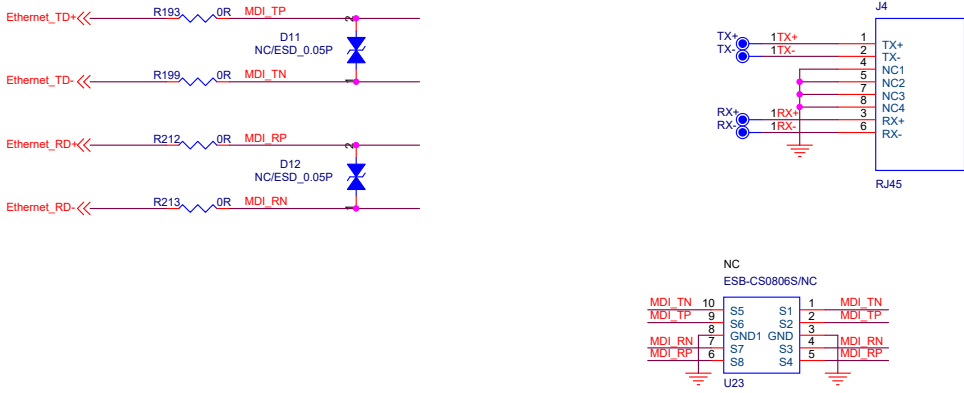
eMMC V5.1

eMMC NC PIN FOR ALLEGRO

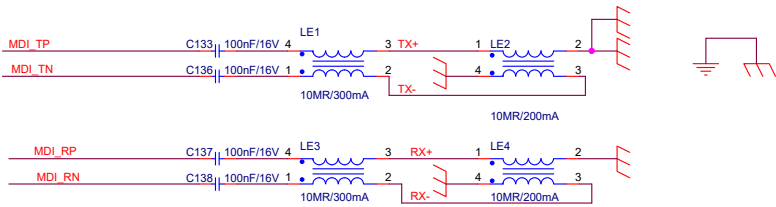
EMMC NET



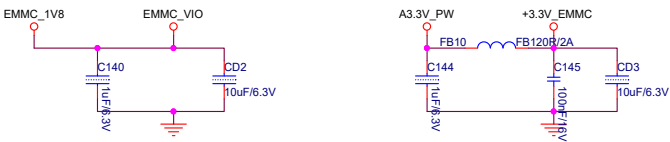
Ethernet Connetor



ENTHERNET 分立

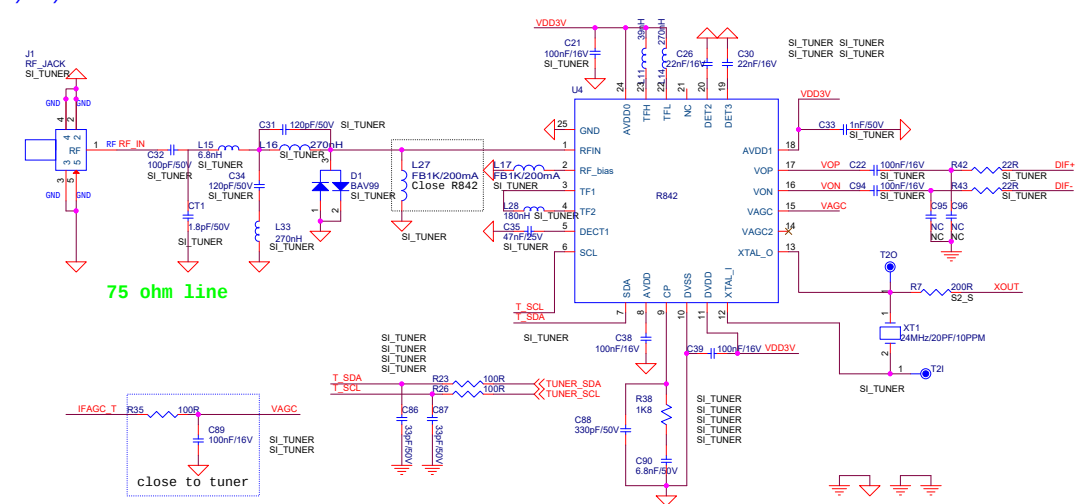


EMMC Power

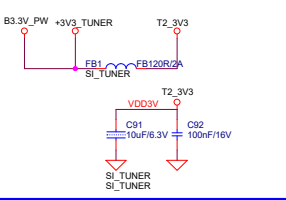


Cultraview		Title	
		CV72690-N42	
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A3		10. EMMC/ENTHERNET	
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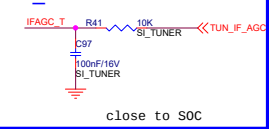
T/T2/C TUNER



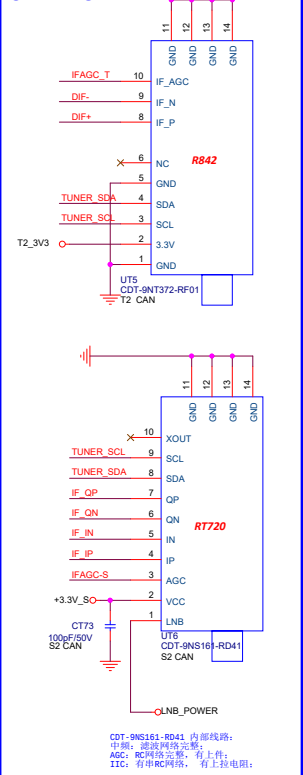
T2 Tuner Power



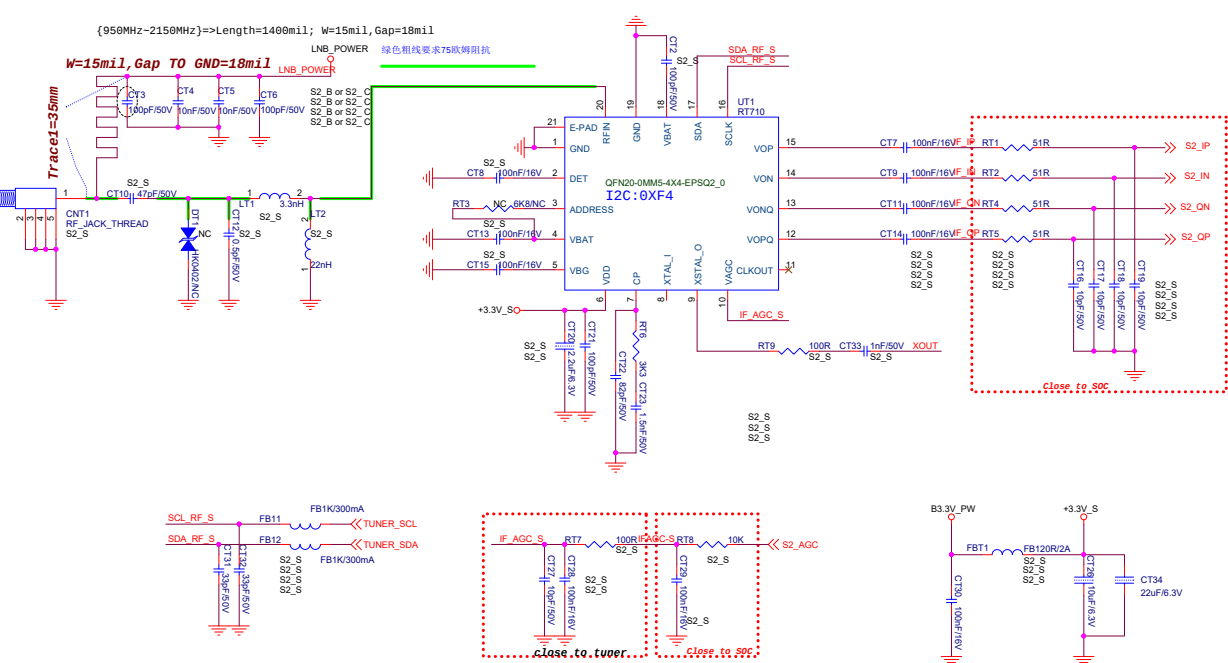
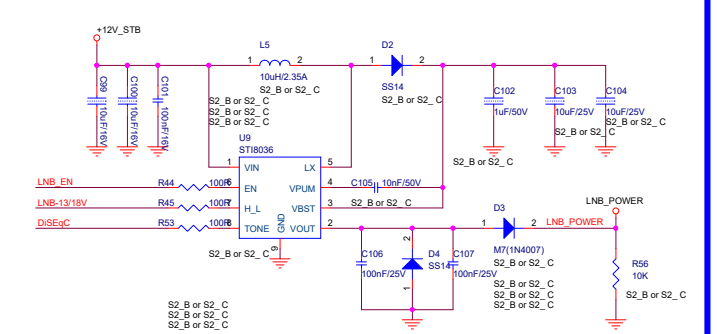
T2 AGC



CAN TUNER

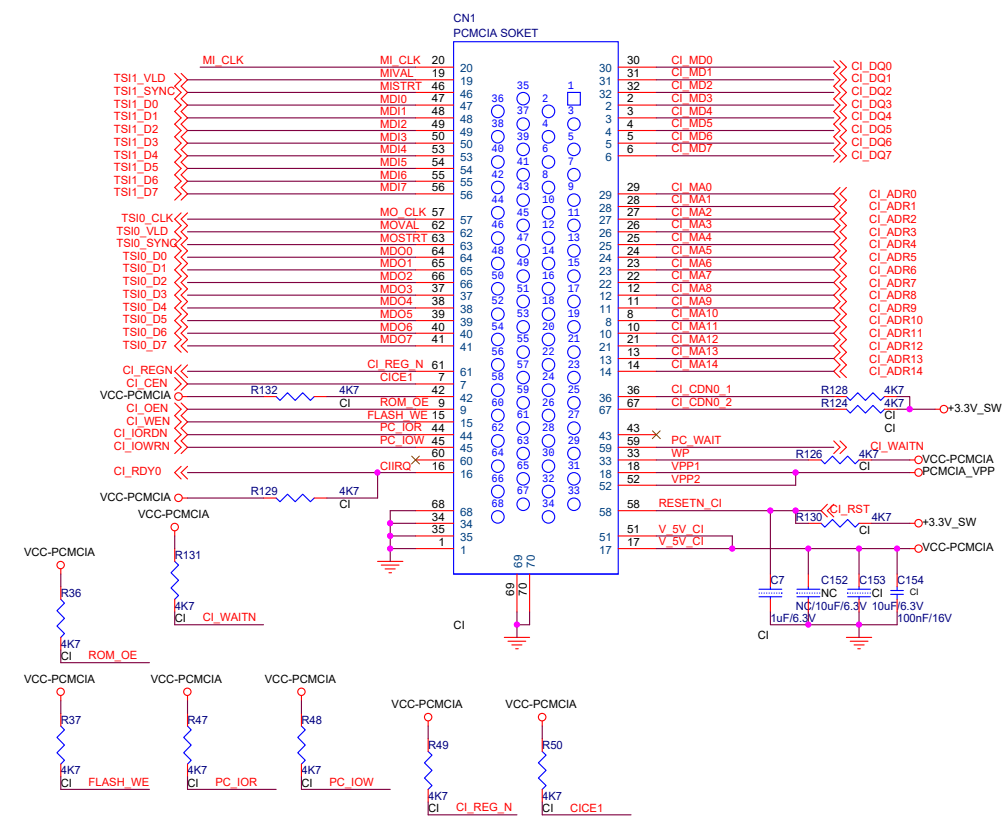


S2 TUNER

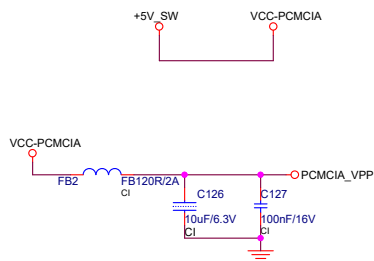
**LNB POWER**

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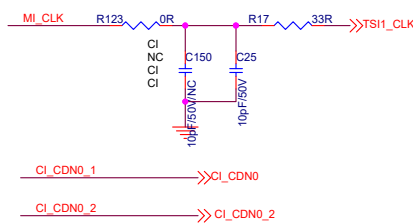
CI Socket



PCMCIA POWER



CLK



[illegible]

POWER

The diagram illustrates the power supply for the CA24 module. A +12V_STB input is connected to a red wire labeled PVDD. This PVDD line also serves as the AMP_POWER output. A CA24 capacitor (470uF/16V) is connected between the PVDD line and GND to provide decoupling.

The circuit diagram shows the HP_MUTE control logic. It features a +3.3V_SW supply connected through a 4K7 resistor (R4) to the HP_EN pin of the Q1201 MOSFET. The HP_MUTE signal is connected through a 10K resistor (R6) to the gate of the MOSFET. A pull-down network consists of two parallel paths from the gate to GND: one through a 4K7NFC capacitor (RA22) and another through a 10K resistor (RA21). The MOSFET's source is grounded, and its drain is connected to the HP_F16 output.

MUTE

AMP_MUTE
0 MUTE
1 NORMAL

AMP_MUTE

RA10 4K7 AMP_EN

RA11 4K7

EARPHONE

J7

GND 1
Audio_B 3
5
4
Audio_E 2

PJ-328T
<FUNCTION>
Earphone Detect
W: Pull Out Earphone;
L: Insert Earphone;

EAR_ROUT EAR_DET +3.3V_SIW

EAR_ROUT EAR_DET

EAR_LOUT 1

CA3 CA8
22nF/16V 22nF/16V

RA23 47K

RA26 1K

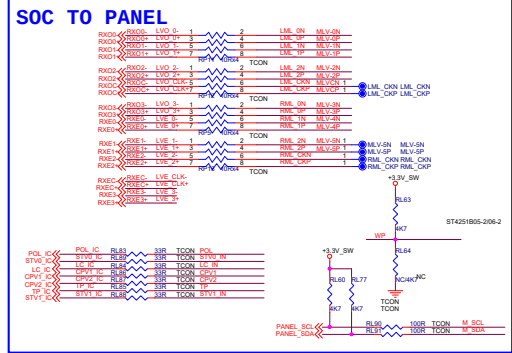
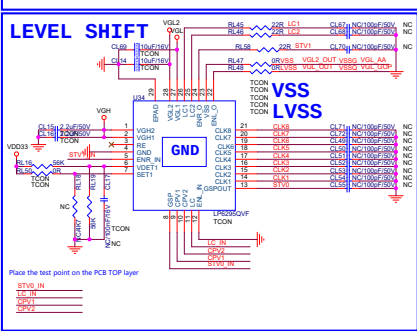
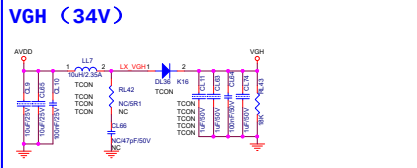
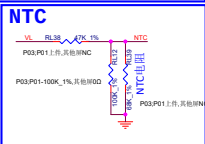
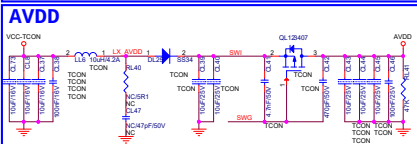
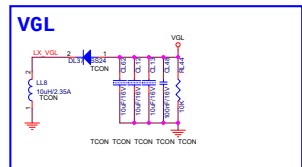
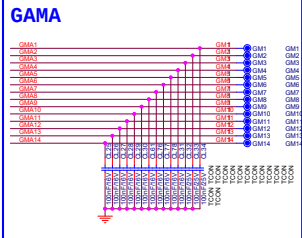
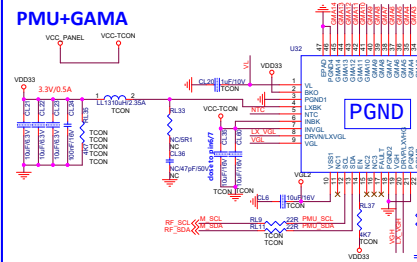
R11 4K7

Q13 3904

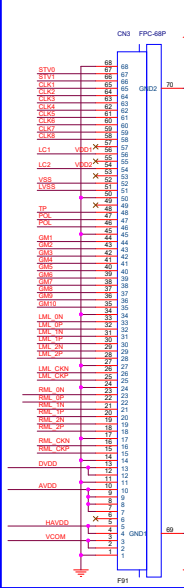
IDENT_HP

R84 4K7/NC

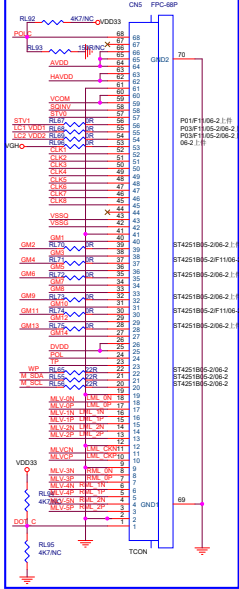
NC



TCONLISS BOE-F91



TCONLISS ST4251B05-2 P01/P03/F11



PANEL TEST POINT

